

## **AMENDMENTS TO THE CLAIMS**

The following listing of claims will replace all prior versions and listings of claims in the application.

### **LISTING OF CLAIMS**

1. (Previously Presented) A program logic device comprising:

a control processor operating according to a high speed clock, the high speed clock obtained by multiplying a standard clock;

input means for inputting signal information into the control processor; and

output means for outputting signal information from the control processor as a signal, wherein

while the control processor is executing a plurality of processings according to the high speed clock, the control processor performs an operation according to signal information that is captured from the input means synchronously with the standard clock and a value of the output means is changed by the control processor within one cycle of the standard clock.

2. (Currently Amended) A program logic device comprising:

a control processor operating according to a high speed clock, the high speed clock obtained by multiplying a standard clock;

input means for inputting signal information into the control processor; and

output means for outputting signal information from the control processor as a signal, wherein

while the control processor is executing a plurality of processings according to the high speed clock, the control processor performs an operation according to a value of signal information that is captured from the input means synchronously with the standard clock and the control processor selectively utilizes a delay function in order to change a value of the output means ~~is changed by the control processor~~ synchronously with the standard clock and within a predetermined number of cycles of the standard clock, the predetermined number of cycles being configurable by the control processor.

3. (Original) A program logic device according to claim 1, wherein

the value of said output means is changed synchronously with said standard clock.

4. (Original) A program logic device according to claim 1, wherein

said control processor has a delay function to synchronize with said standard clock and conducts a next processing after waiting for a predetermined transition of the standard clock.

5. (Original) A program logic device according to claim 1, wherein  
the control conducted by said control processor is determined according to  
the value of the signal captured by said input means synchronously with said standard  
clock.

6. (Original) A program logic device according to claim 1, wherein  
the program logic device comprises:  
comparison value storage means for storing a predetermined comparison  
value in advance; and  
a comparator for comparing the comparison value with the value of the  
signal captured by said input means synchronously with said standard clock, and  
wherein  
a control content of said control processor is determined according to a  
comparison result of the comparator.

7. (Original) A program logic device according to claim 1, wherein  
the program logic device comprises:  
comparison value storage means for storing a predetermined comparison  
value in advance;  
preprocessing means for performing an arithmetic operation of the value  
of the signal captured by said input means synchronously with said standard clock, and  
for setting the value of the signal; and  
comparison means for comparing the comparison value with the value set  
by the preprocessing means, and wherein  
a control content of said control processor is determined according to a  
comparison result of the comparator.

8. (Previously Presented) A program logic device according to claim 1,  
wherein  
after waiting for a value of the signal information that is captured from said  
input means synchronously with said standard clock to become a predetermined value,  
said control processor performs an operation according to the predetermined value.

9. (Original) A program logic device according to claim 8, wherein  
a wait state is released when the number of cycles of said standard clock  
reaches a predetermined number after the wait state.

10. (Original) A program logic device according to claim 8, wherein  
a wait state is released by controlling said control processor for itself.
11. (Original) A program logic device according to claim 8, wherein  
a wait state is released when the value of the signal captured by said input  
means becomes a predetermined value.
12. (Original) A program logic device according to claim 1, wherein  
an interrupt synchronous with the standard clock is generated to said  
control processor according to the value of the signal captured by said input means  
synchronously with said standard clock.
13. (Original) A program logic device according to claim 1, wherein  
the program logic device comprises:  
comparison value storage means for storing a predetermined comparison  
value in advance; and  
a comparator for comparing the comparison value with the value of the  
signal captured by said input means synchronously with said standard clock, and  
wherein  
an interrupt synchronous with the standard clock is generated to said  
control processor according to a comparison result of the comparator.

14. (Original) A program logic device according to claim 1, wherein  
the program logic device comprises:  
comparison value storage means for storing a predetermined comparison  
value in advance;  
preprocessing means for performing an arithmetic operation of the value  
of the signal fetched by said input means synchronously with said standard clock, and  
for setting the value of the signal; and  
a comparator for comparing the comparison value with the value of the  
signal set by the preprocessing means, and wherein  
an interrupt synchronous with the standard clock is generated to said  
control processor.

15. (Original) A program logic device according to claim 12, wherein  
an interrupted position in said control processor is changed according to a  
comparison result of said comparator.